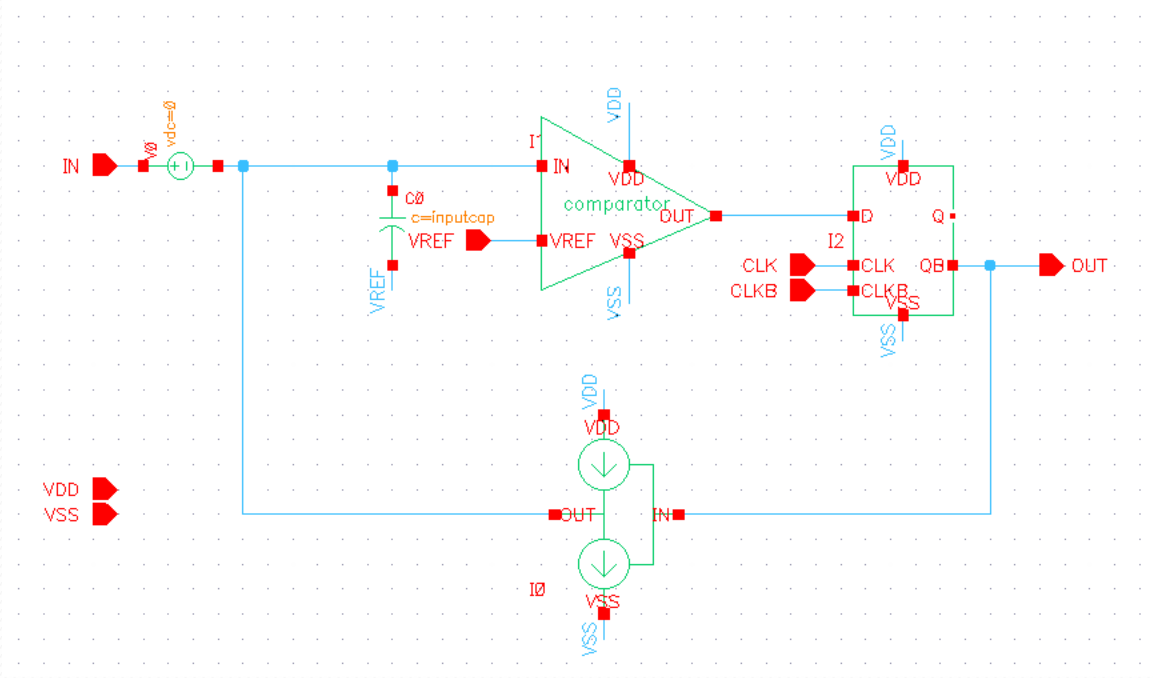
Sigma Delta ADCs

Specifications

- Programmable Sigma-Delta ADC
  - Input sample rate: 48KHz
  - 16bit resolution
    - Switchable to 96KHz@15bits, 192KHz@14bits
- 45nm technology: 1V
- Input current range: ±5μA

Current vs. Voltage Mode

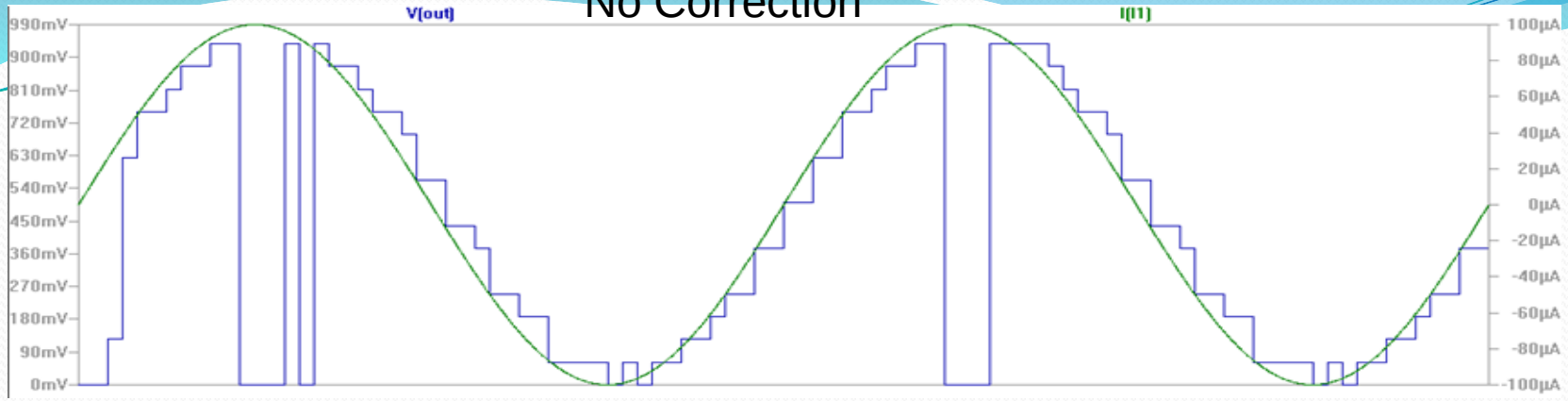
- Input current allows use of capacitor as integrator, rather than op-amp integrator
- Savings in area and complexity
- Requires use of voltage to current converter



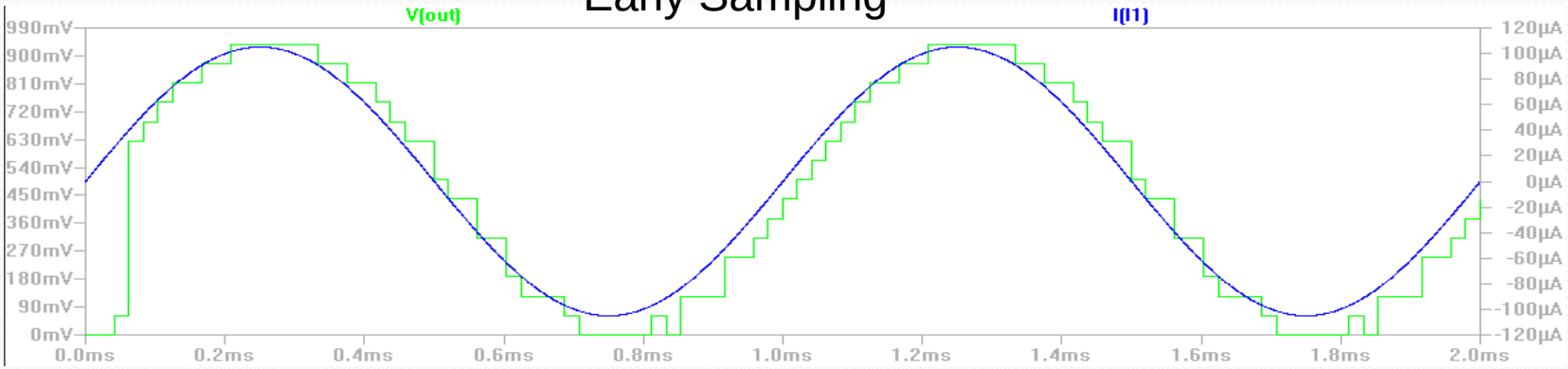
Dealing With Overflow

- 2^n cycles per sampling period, but counter limited to 2^n-1 levels
- Three proposed solutions:
  - Make sure not to overload input
  - Sample before last cycle so overflow never appears at the output
  - Add an overflow bit (requires either an extra bit or one bit less resolution)

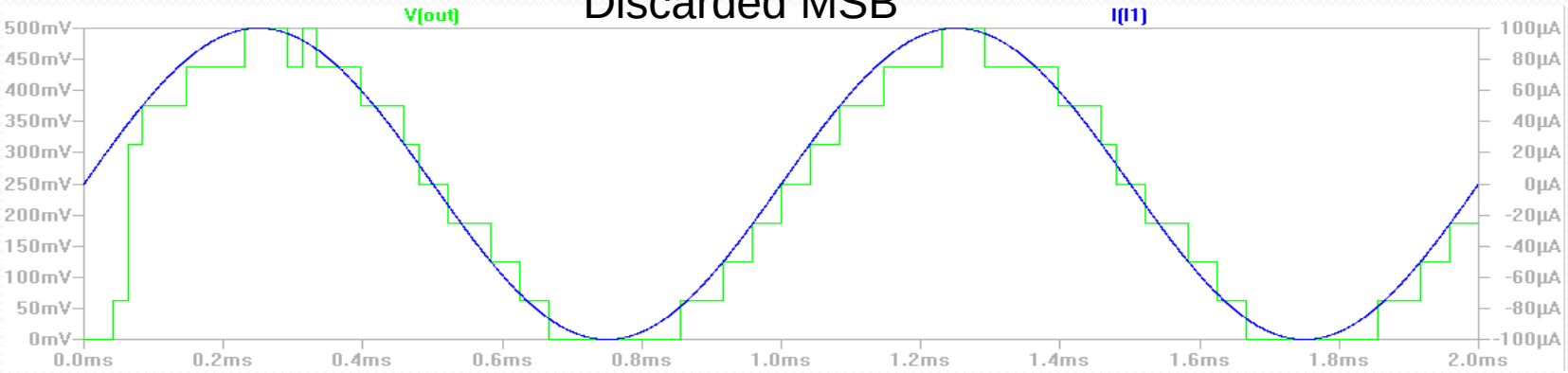
No Correction



Early Sampling



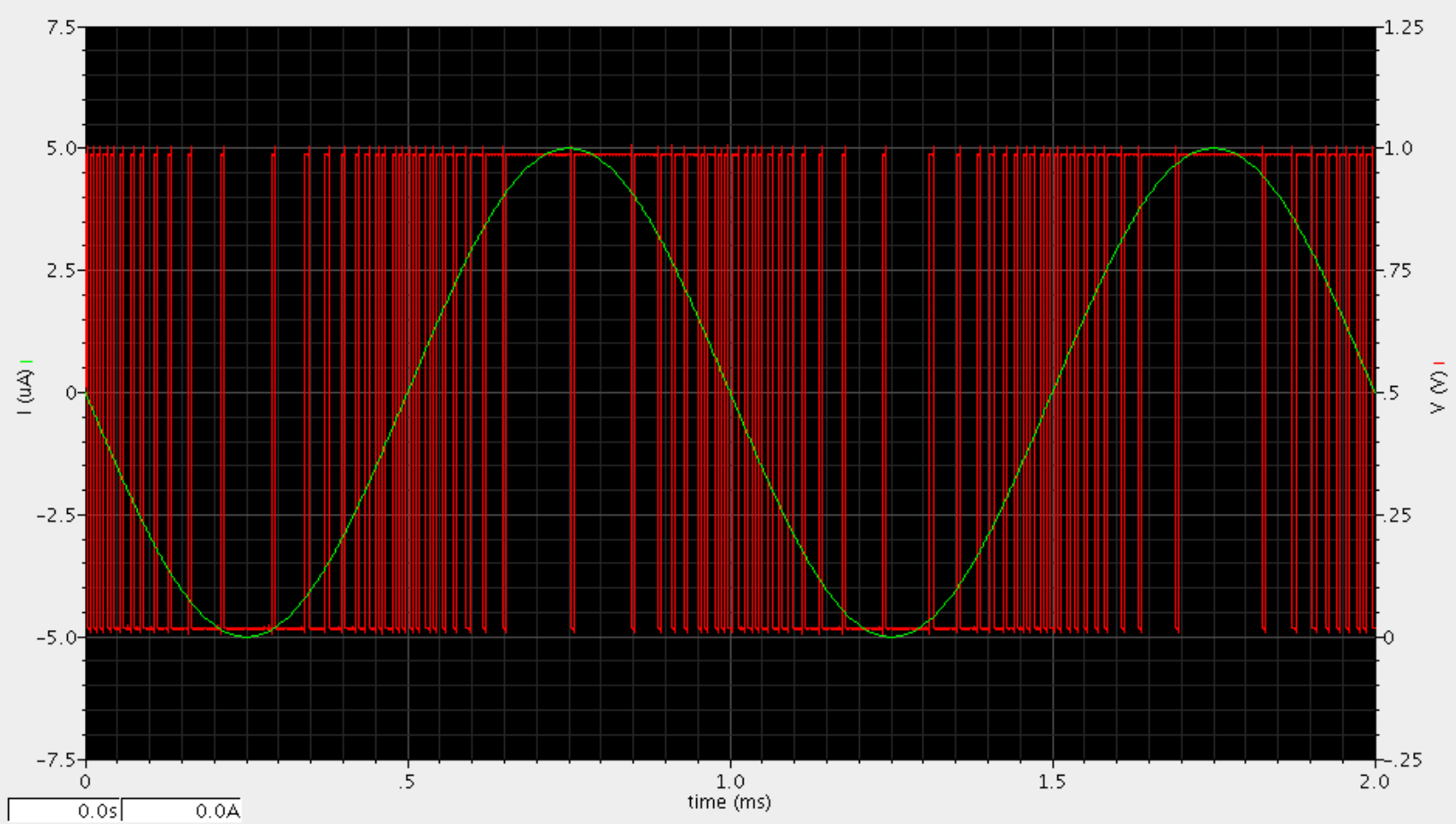
Discarded MSB



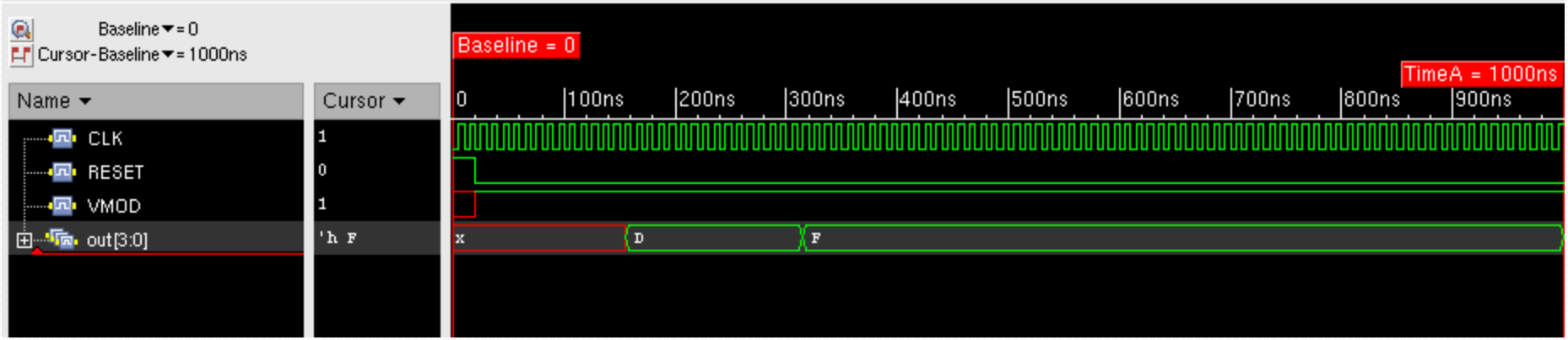
Mixed Signal Synthesis

- Create custom analog cell(s) with standard cell height
- Generate abstract view from layout
- Generate LEF file, append to standard cell LEF file
- Synthesize digital section normally (behavioral Verilog), place and route using timing optimization
- Combine analog and digital circuits using structural Verilog
- Re-run place and route without timing optimization

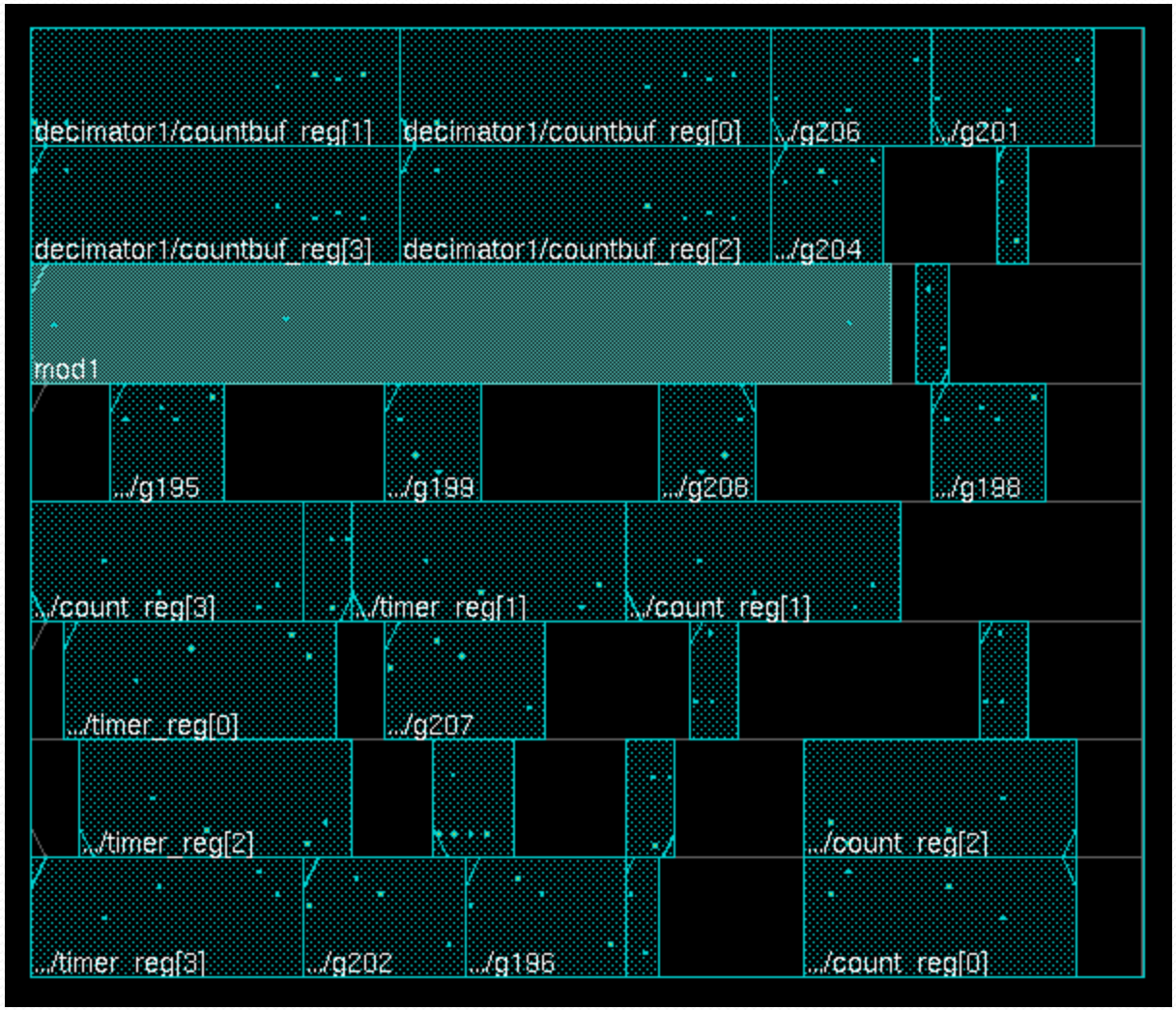
Modulator Output



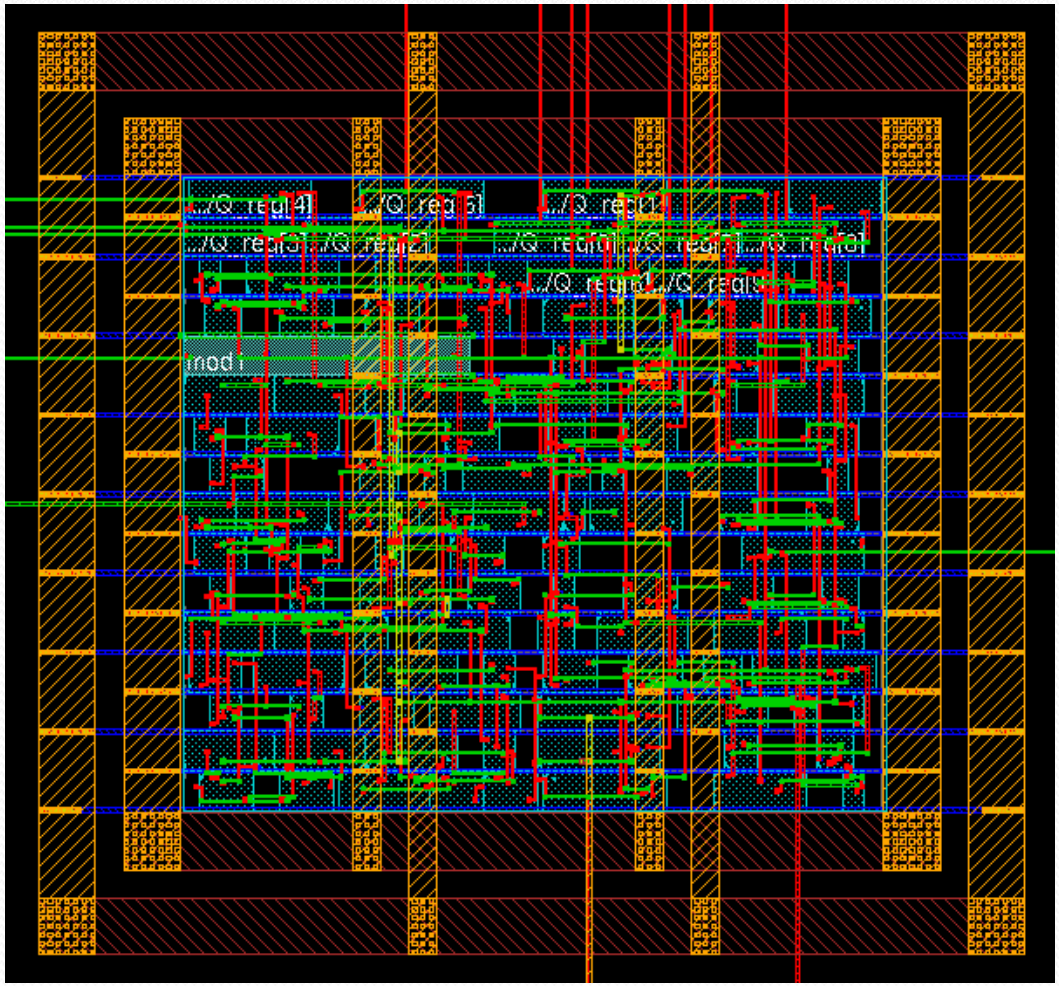
Decimator Simulation



Placed Cells



Placed and Routed



Cell Count and Area

Report Mapped Gates

Generated by: Encounter(R) RTL Compiler v08.10-s222_1 (Mar 25 2009)
Generated on: May 06 2010 01:09:39
Module: decimator16bit
Technology library: NangateOpenCellLibrary revision 1.0
Operating conditions: typical
Interconnect mode: ple

Gate	Instances	Area	Library
AND2_X2	1	1.06	NangateOpenCellLibrary
AND2_X4	15	15.96	NangateOpenCellLibrary
AND4_X1	4	6.38	NangateOpenCellLibrary
DFF_X2	32	144.70	NangateOpenCellLibrary
HA_X1	29	77.14	NangateOpenCellLibrary
INV_X1	2	1.06	NangateOpenCellLibrary
MUX2_X2	1	1.86	NangateOpenCellLibrary
NAND2_X1	2	1.60	NangateOpenCellLibrary
NAND4_X1	1	1.33	NangateOpenCellLibrary
NOR4_X1	1	1.33	NangateOpenCellLibrary
OAI22_X2	1	1.33	NangateOpenCellLibrary
OR3_X2	1	1.33	NangateOpenCellLibrary
OR4_X1	3	4.79	NangateOpenCellLibrary
SDFF_X2	16	97.89	NangateOpenCellLibrary
XOR2_X1	2	3.19	NangateOpenCellLibrary
TOTAL	111	360.95	

Close Help

Analog circuit area of ~15um^2
versus ~500um^2 for full circuit (3%)

Netlist Extraction and Simulation

- OpenAccess for easy management
- Procedure:
  - Extract netlist with Calibre
  - Attach netlist to symbol
  - Simulate with ADE

Programmability

- Oversampling ratio = $\frac{bitstream\_clock}{sample\_rate}$
- With fixed bitstream clock, can trade between sample rate and resolution (through oversampling ratio)

Verilog Code

Decimator Behavioral Verilog

```
module decimator16bit (CLK, VMOD, MODE, Q);
input CLK, VMOD, MODE;
output [15:0] Q;
reg [15:0] count, timer, Q;

  always @(posedge CLK)
    begin
      timer = timer + 1'b1;
      if(timer == 16'hffff && MODE == 1'b0)
                        Q <= count;
      if(timer == 16'h8000 && MODE == 1'b1)
                        Q <= count;
    end

  always @(negedge CLK)
    begin
      if (timer == 16'hffff && MODE == 1'b0)
        count = 16'h0000;
      else if(timer == 16'h8000 && MODE == 1'b1)
        count = 16'h0000;
      else if(VMOD)
        count = count + 1'b1;
      end


endmodule
```

ADC Structural Verilog

```
module adc16bit(IN, CLK, MODE, OUT);
  input IN, CLK, MODE;
  output [15:0] OUT;
  wire IN, CLK, VMOD, MODE;
  wire [15:0] OUT;
  decimator16bit decimator1
     (.CLK (CLK), .VMOD (VMOD), .MODE (MODE), .Q (OUT));
  modulatorL mod1(.IN (IN), .CLK (CLK), .OUT (VMOD));
endmodule
```

Deliverables

- Current mode Sigma Delta modulator schematics
- Programmable decimator verilog code
- Placed and routed ADC layout
- Simulation results and design metrics